SOCIETY FOR ELECTRONIC TRANSACTIONS AND SECURITY [SETS]

CIT Campus, MGR Knowledge City, Taramani, Chennai – 600 113, India.

Advertisement No. SETS/Chn/Rec/Proj/2024-25/35 Date: 12th February 2025

Society for Electronic Transactions and Security [SETS] is a Society under Societies Registration Act, XXI of 1860, dedicated to carryout Research and Development in the field of Information Security focusing on the key verticals, namely, Cryptology and Computing, Hardware Security, Quantum Security and Network Security.

SETS invites applications from citizens of India for filling up the following positions for a Research & Development project in the area of Cybersecurity.:

1. **Project Scientist II & III** - **5 Positions**
2. **Research Associate** - **4 Positions**
3. **Project Associate I** - **2 Positions**
4. **Project Associate II** - **1 Position**

The descriptions of positions, detailed qualification requirements and salary are given below:

1. Project Scientist II & III

Name of the Post	**Project Scientist II & III**
Total Number of Posts	FIVE
Age Limit	Not more than 40 years for Project Scientist II & 45 years for Project Scientist III as on 28.02.2025
Essential Qualification	Doctoral Degree in Science or Master's Degree in Engineering or Technology from a recognized University, degree relevant to domain as in 1.1 or 1.2 or 1.3
Experience	3(Three) to 7(seven) Years of relevant experience Equivalent work experience in lieu of higher degree: - Engineering Doctorates: Four years
Remuneration	All inclusive Consolidated Remuneration would be Rs 80,000 to Rs1,00,000 per month.

1.1 Domain	**Quantum Communication Post Code:25-QSRG-PS-01**
No. of posts for the domain	TWO
Essential Qualification	M.Tech /M.E / MS by Research (Embedded Systems/ Communication Systems/ Quantum Physics/ VLSI Design/ Electrical/ Electronics/ Computer Science/ Information Security/ Cryptography)
Desirable Qualification	PhD in(Embedded Systems/ Communication Systems/ VLSI Design/ Electrical/ Electronics/ Computer Science/ Information Security/ Cryptography) with specialization in Quantum Technologies / Quantum optics/ Quantum Information
Areas of Skill sets/ Knowledge desired	a) Quantum Mechanics & Information Theory & b) Coding Theory in communication c) FPGA programming using Zynq Ultrascale + boards. d) Programming: Python (with Qiskit, Cirq), C++, MATLAB

	e) Quantum Hardware: Experience with photonics and Qantum Optics f) Cryptography & Security (for quantum communication) g) Mathematics: Linear algebra, probability, number theory h) Hardware Side-Channel evaluation i) Electrical Circuits

1.2 Domain	**Quantum Computing Post Code:25-QSRG-PS-02**
No. of posts for the domain	TWO
Essential Qualification	M.Tech /M.E / MS by Research (Computer Science/ Information Theory/ Cryptography and Cybersecurity/ Embedded Systems/ Engineering Physics / Quantum Technologies) or PhD in Mathematics / Applied Mathematics
Desirable Qualification	PhD in (computer Science/ Information Theory/ Cryptography and Cybersecurity/ Embedded Systems/ Engineering Physics / Quantum Technologies) with specialization in in Quantum Technologies / Quantum Information Theory
Areas of Skill sets/ Knowledge desired	a) Programming Experience in C/C++, Python, Linux. b) Quantum Mechanics & Information Theory & c) Programming: Python, C++, MATLAB; Programming quantum computer: Qiskit/ Cirq/ Pennylane/ Braket/ PyQuil/ Liqui /Quantum AI/ QuTiP d) Quantum Hardware: Experience with photonics and qantum optics e) Cryptography & Cybersecurity f) Mathematics: Linear algebra, probability, number theory g) Machine Learning & AI (for quantum)

1.3 Domain	**Hardware Post Code:25-QSRG-PS-03**
No. of posts for the domain	ONE
Essential Qualification	M. Tech /M. E in Electronics & Communication/ Electrical /Applied Electronics/VLSI Design /Embedded Systems
Desirable Qualification	PhD in Electronics & Communication/ Electrical /Applied Electronics/VLSI Design /Embedded Systems
Areas of Skill sets / Knowledge desired	a) Knowledge of hardware components like Processors, Memory, Peripherals and storage devices b) Knowledge of various communication protocols for interfacing between devices c) Knowledge in RISC V Instruction Set Architecture (ISA) d) Hands-on experience in FPGA programming over SoC architecture. e) Knowledge in Linux, including Kernel development and Secure Boot mechanisms.

2. Research Associate

Name of the Post	Research Associate
Total Number of Posts	FOUR
Age Limit	Not more than 40 years as on 28.02.2025
Essential Qualification	60% or above in M.Tech / M.E/ MS in relevant domain as in 2.1 or 2.2
Experience	3(Three) 5(five) Years of Relevant Experience Equivalent work experience in lieu of higher degree: - Engineering Doctorates: Four years
Remuneration	All inclusive Consolidated Remuneration would be Rs 70,000 to Rs 85,000 per month

2.1 Domain	Quantum Communication Post Code:25-QSRG-RA-01
No. of posts for the domain	TWO
Essential Qualification	M.Tech /M.E / MS by Research (Embedded Systems/ Communication Systems/ Quantum Physics/ VLSI Design/ Electrical/ Electronics/ Computer Science/ Information Security/ Cryptography)
Desirable Qualification	PhD in(Embedded Systems/ Communication Systems/ VLSI Design/ Electrical/ Electronics/ Computer Science/ Information Security/ Cryptography) with specialization in Quantum Technologies / Quantum optics/ Quantum Information
Areas of Skill sets/ Knowledge desired	a) Quantum Mechanics & Information Theory & b) Coding Theory in communication c) FPGA programming using Zynq Ultrascale + boards. d) Programming: Python (with Qiskit, Cirq), C++, MATLAB e) Quantum Hardware: Experience with photonics and Qantum Optics f) Cryptography & Security (for quantum communication) g) Mathematics: Linear algebra, probability, number theory h) Hardware Side-Channel evaluation i) Electrical Circuits

2.2 Domain	Quantum Computing Post Code:25-QSRG-RA-02
No. of posts for the domain	TWO
Essential Qualification	M.Tech /M.E / MS by Research (Computer Science/ Information Theory/ Cryptography and Cybersecurity/ Embedded Systems/ Engineering Physics / Quantum Technologies) or PhD in Mathematics / Applied Mathematics
Desirable Qualification	PhD in (computer Science/ Information Theory/ Cryptography and Cybersecurity/ Embedded Systems/ Engineering Physics / Quantum Technologies) with specialization in in Quantum Technologies / Quantum Information Theory
Areas of Skill sets/ Knowledge desired	a) Programming Experience in C/C++, Python, Linux. b) Quantum Mechanics & Information Theory & c) Programming: Python , C++, MATLAB; Programming quantum computer: Qiskit/ Cirq/ Pennylane/ Braket/ PyQuil/ Liqui /Quantum AI/ QuTiP d) Quantum Hardware: Experience with photonics and qantum optics e) Cryptography & Cybersecurity f) Mathematics: Linear algebra, probability, number theory g) Machine Learning & AI (for quantum)

3. Project Associate-II &Project Associate-I

3.1 Domain	**Hardware Post Code:25-QSRG-PA-02**
Name of the Post	**Project Associate-II &Project Associate-I**
Number of Posts	THREE (2 Nos. -PA I; 1No. -PA II)
Age Limit	Not more than 35 years as on 28.02.2025
Essential Qualification	Degree in Engineering or Technology (Electronics & Communication/ Electrical /Applied Electronics/VLSI Design /Embedded Systems) with 60% or above marks or equivalent. (or) Masters in Engineering / Technology (Electronics & Communication/ Electrical /Applied Electronics/VLSI Design /Embedded Systems)
Areasof Skill sets/ Knowledge required	a) Knowledge of hardware components like Processors, Memory, Peripherals and storage devices b) Knowledge of various communication protocols for interfacing between devices c) Knowledge in RISC V Instruction Set Architecture (ISA) d) Hands-on experience in FPGA programming over SoC architecture. Knowledge in Linux, including Kernel development and Secure Boot mechanisms.
Experience	2 Years of relevant experience will be considered as Project Associate-II
Remuneration	All inclusive Consolidated Remuneration would be Rs. 40,000/- to Rs.50,000/- per month.

The positions of **Project Scientist II & III, Research Associate, Project Associate-II & I** as proposed is purely temporary and would be filled on a contract basis with a salary under project mode. The duration of the assignment is initially for a period of One Year and would be extended further based on the need of the project and performance. There is no scope of continuation / regularization/ absorption under any circumstances.

Application Procedure:

Name of the Post	Domain	Post code
1. Project Scientist II & III	Quantum Communication	25-QSRG-PS-01
	Quantum Computing	25-QSRG-PS-02
	Hardware	25-QSRG-PS-03
2. Research Associate	Quantum Communication	25-QSRG-RA-01
	Quantum Computing	25-QSRG-RA-02
	Hardware	25-QSRG-RA-03
3.Project Associate II & I	Hardware	25-QSRG-PA-02

1. The candidate is requested to attach the following documents: -
    a. Scanned copies of academic certificates (Single PDF document)
    b. Scanned copies of Experience certificates (Single PDF document)

3. The last date for uploading applications is 28.02.2025 before 6 PM.

4. Shortlisted candidates would be required to attend a Written Test and/or Interview at SETS, Chennai. The date and time for this would be intimated to shortlisted candidates by E-mail.

Terms and Conditions:

1. The shortlisted candidates would be required to bring all their original testimonials for verification on the interview day.

2. No TA/DA will be given to candidates appearing for interview.

3. The prescribed qualifications are minimum and mere possession of the same does not entitle the candidate to be called for the written test or interview. The decision of the Executive Director of SETS in all matters relating to eligibility, acceptance or rejection of the applications, cancellation of advertisement and filling up or not filling up of post will be final and no inquiry or correspondence will be entertained in this matter.

4. Number of vacancies may increase/decrease depending upon SETS requirements and such changes will be made by SETS without any notice

Executive Director